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### Boolean and Elementary Algebra with a Roll-To-Roll Printed Electrochemical Memristor

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#### ABSTRACT

A non-volatile conjugated polymer-based electrochemical memristor (cPECM), derived from sodium 4-[(2,3-dihydrothieno[3,4-b][1,4]dioxin-2-yl)methoxy] butane-2-sulfonate (S-EDOT), is fabricated through roll-to-roll printing and exhibited neuromorphic properties. The 3-terminal device employed a "read" channel where conductivity of the water-soluble, self-doped S-PEDOT is equated to synaptic weight and was electrically decoupled from the programming electrode. For the model system, a +2500 mV programming pulse of 100 ms duration resulted in a 0.136  $\mu$ S resolution in conductivity change, giving over 1000 distinct conductivity states for one cycle. The minimum programming power requirements of the cPECM was 0.31 pJ mm<sup>-2</sup> and with advanced printing techniques, a 0.1 fJ requirement for a 20  $\mu$ m device is achievable. The mathematical operations of addition, subtraction, multiplication, and division are demonstrated with a single cPECM, as well as the logic gates AND, OR, NAND, and NOR. This demonstration of a printed cPECM is the first step toward the implementation of a mass produced electrochemical memristor that combines information storage and processing and may allow for the realization of printable artificial neural networks.

Keywords: conjugated polymer, low-power programming, S-PEDOT

#### 1. Introduction

Inorganic/organic memristors have experienced vigorous research activity since 2008 with the verified existence of Chua's 1971 proposed fourth basic element.<sup>[1,2]</sup> Nonetheless, the majority of memristive systems rely on some form of a stochastic creation/disruption of percolative paths inside a matrix to

give rise to a binary (or abrupt) form of current switching. These systems were predominately developed to serve as a memory component in a von Neumann computer architecture<sup>[3]</sup> and have, especially in the case of inorganic systems, proven to be suitable for storing and processing information with numerous excellent attributes.<sup>[2]</sup>

The memory requirements for a von Neumann computer architecture differ greatly from biologically inspired synaptic functions, where synaptic weights are modulated by the number and frequency of homogeneous spikes and take a continuity of values. A number of review papers<sup>[4-8]</sup> have been presented that focus on memristors intended for neu-romorphic applications and all share the common theme, that in this role, mem-ristors must exhibit reliable analog properties including non-abrupt switching transitions, continuously variable resistance states, and a predictable response. Compared to their inorganic counterparts, organic materials have several advantages when it comes to fabrication and implementation as a neuro-morphic device. Organic materials can be integrated to large-scale production with low-cost manufacturing processes and high resolution lithography patterning along with tailoring the chemistry to desired chemical, electrical and mechanical properties.<sup>[7,8]</sup> These traits allow memristor devices to provide a simple and effective route for fabricating physical artificial neural networks which are independent of software programming.<sup>[9,10]</sup>

Over the past few decades, organic electrochemical transistors (OECTs) have been explored as potential bioelec-tronics,<sup>[11,12]</sup> printed circuits<sup>,[13]</sup> and neuromorphic devices.<sup>[8,14,15]</sup> A recent embodiment of an OECT was a non-volatile conjugated polymer-based electrochemical memristor (cPECM) that exhibited characteristics of an artificial synapse and could be useful for neuromorphic computing.<sup>[14]</sup> In this 3-terminal device, the redox state and conductivity of poly(3,4-ethylenedioxythiophene) :poly(4-styrenesulfonate) (PEDOT:P S S) between two terminals was controlled by a third terminal, which allowed the state of conductance to be decoupled from the barrier for changing states. Neuromorphic devices based on electrochemical materials, such as PEDOT:PSS, have been shown to emulate essential artificial neuronal and synaptic plasticities for learning and memory behaviors,<sup>[14,16-19]</sup> though other conjugated polymers have also been utilized. For example, synapse-like behavior was demonstrated by a three-terminal light-stimulated organic field-effect transistor (OFET) which employed a p-type donor-acceptor conjugated polymer channel(poly(thienothiophene-co-1,4-diketopyrrolo[3,4-c]pyr-role) (PDBT-co-TT)) doped with an ionic additive (tetrabutylam-monium perchlorate (TBAP)).<sup>[20]</sup>

PEDOT:PSS has achieved widespread implementation into a host of organic devices due to its electrical conductivity and commercial availability as an aqueous dispersion of colloidal particles.<sup>[21-23]</sup> Specifically, PEDOT:PSS exhibits high electrical conductivity (1000 S cm<sup>-1</sup>) coupled with optical transparency and has been exploited in a wide range of applications where a transparent conductive electrode is desirable and indium tin oxide is not preferred.<sup>[24,25]</sup> Nonetheless, PEDOT:PSS has various technical issues that present challenges in its application. These issues largely stem from the use of PSS as external ions to compensate the positive charges on PEDOT. To achieve a water dispersible system, a hydrophobic PEDOT core is coated with a shell of excess hydrophilic PSS, yielding a colloidal particle with a diameter of several tens of nanometers,<sup>[24]</sup> which presents difficulties in forming layers thinner than the colloidal particle size.<sup>[26]</sup> In addition, the neat PEDOT:PSS dispersion requires a number of additives (e.g., ethylene glycol, dimethyl sulfoxide, and sorbitol) to achieve high levels of conductivity.<sup>[27-29]</sup> While these additives are known to improve the film's conductivity, they can create a more complex processing parameter inter-relationship and present challenges to achieving highly uniform printed films.<sup>[30]</sup>

A key advantage of conductive polymers is their amenability to being printed into devices, where various printing techniques have been demonstrated. <sup>[31-33]</sup> Printing is a process which converges in on

traditional manufacturing techniques with the advent of functional, processable nanoscale materials.<sup>[32]</sup> The art is rapidly becoming a science and inherently demonstrates a vast range of scalability from nearly microscopic to incredibly large and high-throughput, with a specific implementation being roll-to-roll (R2R) printing. R2R printing techniques have been employed in the creation of a range of electronic devices,<sup>[34]</sup> such as large area photovoltiac devices,<sup>[21,35]</sup> memory devices,<sup>[36]</sup> and sensors.<sup>[33]</sup> Recent advances in R2R printing achieved structures with a minimum internal linewidth of 3 µm at print speeds of 0.2 m s<sup>-1</sup>.<sup>[37]</sup> Continued developments in printing electronic devices with a smaller feature size at higher printing speeds will require the development of semiconducting polymers that exhibit both high intrinsic conductivities and charge carrier mobilities without the need of additives prior to being formulated in printable "inks".<sup>[32]</sup> To that end, a recently presented water-soluble self-doped PEDOT (S-PEDOT) with an electrical conductivity as high as 1089 S cm<sup>-1</sup> without use of additives<sup>[38]</sup> was employed in the current effort in the R2R printing of a flexible cPECM.

#### 2. Results and Discussion

**Figure 1**a presents a schematic of the cPECM sandwich device. The top layer forms the presynaptic electrode, which is composed of a conjugated polymer layer that sits atop of an electrolyte layer, which in turn sits atop a layer composed of the conjugated polymer and polyethyleneimine (PEI). The latter layer forms the postsynaptic electrode where a (D)rain and (S)ource electrode are attached to it. A synaptic weight is equated to the conductivity of the channel (i.e., oxidation state of S-PEDOT) between the D and S electrode, while the conductivity of the channel is programed through voltage pulses (synaptic events) to the (G)ate electrode attached to the presynaptic layer.

In the current embodiment of a cPECM, the self-doped and water-soluble form of poly(3,4ethylenedioxythiophene) (PEDOT) is employed in the construction of the device, namely S-PEDOT (cf. Figure 1b). This conjugated polymer is synthesized from the monomer sodium 4-[(2,3dihydrothieno[3,4-b][1,4]dioxin-2-yl)methoxy]butane-2-sulfonate (S-EDOT), a novel EDOT derivative bearing a sodium alkylsulfonate side chain.<sup>[38]</sup> The presynaptic layer is composed of S-PEDOT, while the postsynaptic layer is composed of S-PEDOT and a vapor-deposited PEI. PEI is an alkyl chain with primary, secondary, and tertiary amines and only a portion of the amines of PEI are typically protonated. This results in PEI having a high proton buffering capacity. PEDOT has been indicated to have an inherent nature to oxidize with ambient oxygen<sup>[39,40]</sup> and its oxidation within a device will impede on state retention, cycle stability, and overall device performance for longterm applications.<sup>[15,41]</sup> The use of PEI with PEDOT has been shown to stabilize the PEDOT, with PEI acting as a reductant by donating electrons to the oxidized PEDOT.<sup>[42]</sup> This process assists in stabilizing the neutral form of S-PEDOT and, with the electron blocking nature of the poly(ethylene glycol) (PEG)/tetrabutylammonium hexafluorophosphate (Bu<sub>4</sub>NPF<sub>6</sub>) electrolyte layer, maintain the oxidation state of the postsynaptic layer. With no driving bias applied to the device, the electrolyte prevents any electron recombination reactions by decoupling the electron transfer between the presynaptic and postsynaptic layers.<sup>[14]</sup>

The circuit implemented for programming synaptic events and reading synaptic weights of the cPECM device is presented in **Figure 1**c. The current flowing in the channel between the D and S electrodes  $(i_{ds})$  under a constant DC voltage  $(V_{ds})$  is converted to conductance, which is equated to the synaptic weight of the circuit. To program the device, a potential pulse applied at the G electrode  $(V_g)$  alters the conductance of the channel and synaptic weight of the circuit. Positive voltage pulses  $(+V_g)$  to the G electrode tune the carrier concentration of the S-PEDOT:PEI channel by protonating the PEI by a chain

of events that results in a decrease in channel conductivity, while negative voltage pulses  $(-V_g)$  result in an increase in channel conductivity.



**Figure 1**. a) Sandwich construction of a conjugated polymer electrochemical memristor (cPECM). b) Structure of self-doped poly(3,4-ethylenedioxythio-phene) (S-PEDOT) and polyethyleneimine (PEI). c) Circuit representation for programming and reading the conductance state of cPECM. d) Schematic of a gravure roll-to-roll printing configuration.

The devices were fabricated through a roll-to-roll (R2R) gravure printing process schematically presented in **Figure 1**d. R2R printing refers to a range of manufacturing technologies that involves the continuous processing of a pliant substrate as it traverses between two moving rolls of material. Advances in the R2R manufacturing process have made it the likely candidate for economically producing large format multifunctional systems at scale, such as printed electronics.<sup>[32,33]</sup> The S-PEDOT was dissolved in a 2:1 methanol:water mixture and was deposited at a ca. 0.2 m s<sup>-1</sup> rate onto flexible indium tin oxide (ITO)-coated polyethylene terephthalate (PET) sheets using a commercial proofing R2R printer. Prior to printing, the ITO sheets were templated to form the top G electrode and split D and S electrode assemblies. Once printed, PEI was evaporated onto the postsynaptic layer, the PEG/Bu<sub>4</sub>NPF<sub>6</sub> electrolyte was deposited on the postsynaptic layer, and then the two synaptic layers were mated to form the sandwich structure presented in **Figure 1**a.



**Figure 2**. a) Voltage-driven conductance tuning of S-PEDOT electrochemical memristor depicting 500 distinct states per potentiated or depressed cycle. The gate electrode is programmed with a 500 ms voltage pulse of ±1000 mV (V<sub>g</sub>) while monitoring the drain current i<sub>ds</sub> with a channel voltage -100 mV (V<sub>ds</sub>). b) Current-driven conductance tuning of electrochemical memristor depicting 10 potentiated and depressed conductivity states per cycle.

Figure 2a presents the multitude of conductive states, or synaptic states, available to the cPECM when programmed with voltage pulses. In this curve, a single programming step is a square-wave pulse with a ±1000 mV magnitude of 500 ms duration followed by a 500 ms 0 mV period which is applied to the G electrode ( $V_e$ ). Each full cycle consists of 500 steps of the +1000 mV pulse followed by 500 steps of a -1000 mV pulse. During the programming cycles, a current read across the channel is made every 66 ms from a potential of -100 mV (V<sub>ds</sub>) applied across the D and S electrodes. The channel conductance  $(\sigma)$  between 30 x 10<sup>3</sup> and 100 x 10<sup>3</sup> read measurements is presented in **Figure 2** to demonstrate the reproducibility of the device, where the total differential in conductance from peak maximum to minimum is ca. 68  $\mu$ S. The changes in conductance between successive programming steps is relatively linear for the first few hundred pulses, but as the the S-PEDOT approaches a "fully" oxidized or reduced state, the system becomes saturated and the changes in conductance begin to diminish between successive impulses. As indicated earlier, a positive potential during a programming operation results in the movement of a cation (proton) from the presynaptic layer through the electrolyte layer into the postsynaptic layer where it protonates the PEI. For charge neutrality, electrons flow from the external circuit into the postsynaptic layer reducing the S-PEDOT, resulting in a decrease in  $\sigma$  of the channel and an increase in the observed current flow. During the "read" operation, a constant value of  $\sigma$  was observed at the new conductance level and was stable for a 24 minute observation period with a 0.0175% (0.040  $\mu$ S) decrease over this time. This process was reversible, where a subsequent train of opposite voltage pulses returns the device to its initial conductance. Similarly, Figure 2b presents the tuning of the channel through 10 poten-tiated/depressed states with the substitution of V<sub>g</sub> (cf. Figure 1c) with a current source and employing a square-wave current pulse of  $\pm 1 \,\mu$ A for 500 ms. In this case, current flowing out of the G electrode results in cations flowing from the postsynaptic layer to the presynaptic layer and increases the conductivity of the channel. From Figure 2b, the linear change in conductance between each successive current pulse is clearly discernible.

The specific conductivity state of the channel can be tuned by varying the duration and/or amplitude of the applied square-wave voltage (or current) pulse since the oxidation state of the S-PEDOT in the postsynaptic layer is a function of the total charge that is transferred in or out of this layer. Remembering that a positive voltage pulse to the G electrode resulted in a decrease in the channel conductance and that positive and negative voltage pulses of equal magnitude result in the same absolute conductance change, **Figure 3**a,b presents the change in conductance of the channel with increases in voltage pulse amplitude and duration, respectively. A linear trend in the increase of the

absolute value of  $\Delta \sigma$  is evident by increasing pulse amplitude as well as duration. For example, with a +2500 mV pulse of 100 ms duration, a 0.136  $\mu$ S resolution in conductance change is realized. A pulse magnitude of +2500 mV insured charge flow for short pulse durations. The predictable increase is a direct result of the linear change in the number of cations that depart the presynaptic electrode with a positive voltage pulse.



Figure 3. The change in channel conductance of the cPECM as a function of a) pulse amplitude with a 500 ms duration and b) pulse duration with a +2500 mV amplitude (inset presents shorter time regime). c) Paired-pulse facilitation (PPF) of the cPECM with a pair of square-wave V<sub>g</sub> pulses (+1000 mV, 500 ms) separated by a time interval (Δt).

A similar trend is seen when voltage pulses with a negative amplitude are employed. The linearity in conductivity changes of the cPECM to differing parameters of the voltage pulses to the gate electrode affords a simplicity in devising sophisticated decision responses which will be discussed later concerning Boolean algebra.

The mechanism of the cPECM to read, write, and erase is akin to that of the human nervous system. With the gate and channel electrodes mimicking that of the pre- and postsynapses, the synaptic weight is modulated based on the current flow through the doped conjugated polymer channel. Paired-pulse facilitation (PPF), a biological mechanism in the short-term plasticity regime, was used to demonstrate the neuromorphic functionality of the S-PEDOT cPECM. PPF is a phenomena that measures the response characteristics between two biological stimuli (in this case, electrical pulses) based on the timescale between the pulses being fired ( $\Delta$ t) and is presented in **Figure 3**c. A pair of square-wave V<sub>g</sub> pulses (+1000 mV, 500 ms) separated in time from 40 ms to 5000 ms ( $\Delta$ t) were applied to the device while monitoring the channel current ids at a constant V<sub>ds</sub> (-100 mV). The absolute value of the

difference in the observed conductivities ( $|\Delta\sigma| = |\sigma_2 - \sigma_1|$ ) for a set of paired pulses was employed in evaluating the PPF relationship.

The PPF response was modeled with a dual exponential of the form:

$$PPF = C_1 \exp(t/\tau_1) + C_2 \exp(t/\tau_2)$$
(1)

and gave values for  $\tau_1$  and  $\tau_2$  of 13.34 ms and 518.0 ms, respectively, with  $C_1 = 0.6536$  and  $C_2 = 0.2208$ . The S-PEDOT cPECM displays a rapid phase relaxation of  $\tau_1 = 13.34$  ms and a slow phase relaxation of  $\tau_2 = 518.0$  ms, resulting in a minimal potentiation difference for pulse separations greater than 600 ms (cf. **Figure 3**c). These time characteristics are comparable to that of biological synapses.<sup>[43]</sup> In terms of other cPECM devices, it is speculated for pulse intervals less than the slow phase relaxation time, protons can accumulate at the electro-lyte/channel interface before the second stimuli is applied which does not allow for proper electronic state decoupling. At time scales greater than the slow phase relaxation in a smaller change in postsynaptic current between paired-pulses.<sup>[44]</sup>

Basic capabilities required in a memristor where neuro-morphic properties are desired include the ability to perform elementary algebra. The simplest operations in this field of mathematics include addition, subtraction, multiplication, and division. With the cPECM device, positive voltage pulses increase the channel current and represent addition while negative pulses decrease the channel current and represent subtraction. Figure 4 presents a typical addition and subtraction operation in the form of  $\mathbf{A} - \mathbf{B} = 0$  [+15 + -15 = 0]. A has the numerical value of "+15" and is represented by 15 square-wave +1000 mV, 500 ms pulses applied to the G electrode. The conductivity of the channel increases for each pulse and the current change from the baseline value at the onset of the operation is defined as the percent current change (PCC), where PCC =  $(i - i_{\circ}) \cdot (100/i_{\circ})$ . Each square-wave pulse of the form of +1000 mV and 500 ms duration raises the PCC on average by 0.048%, with 15 pulses, that is, the number "+15", being represented by a PCC value of 0.720%. Applying a square-wave pulse of the form of -1000 mV and 500 ms duration results in a decrease of the PCC on average of 0.048%. The addition of the number "-15" in the form of 15 -1000 mV pulses to the PCC value of 0.720% ("+15") results in a final PCC value of 0.0005%, effectively the number "0". Within our laboratory-bench devices, the variability in PCC values for the representation of "15" from device to device was typically less than  $|\Delta PCC| = 0.01\%$ , though this could be reduced in a true manufacturing environment. In **Figure** 4, the standard deviation for 8 unique arithmetic runs are presented as error bars at each calculation step.



Figure 4. Addition and subtraction: A - B = 0 [+15 + -15 = 0]. Error bars represent standard deviation of 8 unique calculation cycles.



Figure 5. Multiplication as a repeated addition with equal groupings:  $\mathbf{A} \times \mathbf{B} = \mathbf{B} \times \mathbf{A} = \mathbf{C} [3 \times 5 = 5 \times 3 = 15]$ . a)  $3 \times 5$ , b)  $5 \times 3$ , and c)  $3 \times -5$ .

Multiplication is often referred to as repeated addition with equal groupings. Figure 5a,b presents multiplication through the addition of multiple sets of pulses where  $A \times B = B \times A = C$  [3 x 5 = 5 x 3 = 15]. In this case, "3 x 5" implies 3 sets of 5 square-wave pulses (+1000 mV, 500 ms) with a 2000 ms delay between each multiplication set. Upon pulsing the device, "3 x 5" resulted in a PCC of ca. 0.712% while performing "5 x 3" resulted in the same PCC value of 0.712%, demonstrating the associative property in multiplication. In addition, Figure 5c presents A x B where A = 3 and B = -5 and "3 x -5" is represented by 3 sets of 5 negative amplitude square-wave pulses (-1000 mV, 500 ms), giving a final PCC value of -0.712%, or its numerical value of "-15".

Division, that is,  $\mathbf{A} + \mathbf{B} = \mathbf{C}$ , can be demonstrated through a "division as repeated subtraction method"<sup>[45,46]</sup> and is presented for  $\mathbf{A} = 15$  and  $\mathbf{B} = 6$  in **Figure 6**. Initially, the value of the integer quotient  $n_1$  is found that results in the remainder  $(r_1)$  to be  $r_1 < \mathbf{B}$  for  $n = \mathbf{A} - n \cdot \mathbf{B}$ . In the present case,  $n_1 = 2$  satisfies this criteria with  $15 - 2 \cdot 6 = 3$ . The number 15 is initially represented by a PCC value of 0.712%, then 2 groups of 6 negative amplitude pulses (-1000 mV, 500 ms) are applied to the G electrode of the cPECM device. This lowers the PCC value to 0.149%, the numerical equivalent of 3. To find the remainder in a decimal format, the remainder  $(r_1)$  is then replaced by  $r_2 = r_1 + r_1 \cdot 9 = 3 + 27 = 30$ . To achieve this, 3 groups of 9 positive amplitude pulses (+1000 mV, 500 ms) are applied to the G electrode of the cPECM device to raise the PCC to 1.410%, or the numerical equivalent of 30. The successive subtractions with the integer quotient  $(n_2)$  in the decimals place are performed for  $r_3 = r_2 - n_2 \cdot \mathbf{B}$  until  $r_3 = 0$ . If  $r_3 \neq 0$ , repeat  $r_2 = r_1 + r_1 \cdot 9$  and  $r_3 = r_2 - n_2 \cdot \mathbf{B}$  until  $r_3 = 0$ . In the present case,  $n_2 = 5$  satisfies this criteria with  $30 - 5 \cdot 6 = 0$  and the division is complete.



Figure 6. Division as repeated subtraction method:  $\mathbf{A} \div \mathbf{B} = \mathbf{C} [15 \ 6 = 2.5]$ 

To achieve this, 5 groups of 6 negative amplitude pulses (-1000 mV, 500 ms) are applied to the G electrode of the cPECM device to lower the PCC to 0.00003%, or the numerical equivalent of 0. The final quotient (Q) is the sum of the integer quotients  $\rho = n_1 + 0.n_2 = 2 + 0.5 = 2.5$ .

Boolean algebra includes those logic operations that employ Boolean values which take on the values of either TRUE or FALSE, often represented by a *1* and *0*, respectively. Boolean algebra is a vital capability for any memristor that might be used in neuromorphic computing and can be demonstrated for the S-PEDOT-based cPECM with the logic operations of AND, OR, NOR, and NAND, where **Table 1** presents their truth tables.

With a cPECM device, the square-wave voltage pulses sequentially applied to the G electrode have specific amplitudes and durations in order to represent a TRUE or FALSE value within a specific logic gate and are presented in **Table 2**. For example, with the AND gate, a FALSE value is passed to the memristor with a square-wave pulse of -500 mV and 500 ms duration, while a TRUE value is passed as a pulse of +1000 mV with the same duration.

**Figure 7**a presents the AND truth table generated by the cPECM device. The initial state of current in the channel is measured giving a baseline absolute value  $|i_{ds,o}| = 71.188 \ \mu$ A, which is employed in defining future logical outputs of the device. The output logic is configured such that for  $|i_{ds}| > 71.188 \ \mu$ A results in a TRUE output, otherwise, for  $|i_{ds}| < 71.188 \ \mu$ A the output is FALSE. In the cPECM device, the channel conductivity was evaluated by monitoring the current flow in the channel to a -100 mV potential across the D and S electrodes. Therefore, a positive voltage pulse to the G electrode resulted in an increase in the channel current and a decrease in the channel conductivity.

|      |        |   |   | Truth table |   |   |  |
|------|--------|---|---|-------------|---|---|--|
| AND  | Input  | Α | F | Т           | F | Т |  |
|      |        | в | F | F           | т | Т |  |
|      | Output |   | F | F           | F | Т |  |
| OR   | Input  | Α | F | Т           | F | Т |  |
|      |        | в | F | F           | Т | Т |  |
|      | Output |   | F | Т           | т | Т |  |
| NAND | Input  | Α | F | Т           | F | Т |  |
|      |        | В | F | F           | т | Т |  |
|      | Output |   | Т | Т           | т | F |  |
| NOR  | Input  | Α | F | Т           | F | Т |  |
|      |        | В | F | F           | т | Т |  |
|      | Output |   | т | F           | F | F |  |

Table 1. Truth table for AND, OR, NAND, and NOR logic gates.

**Table 2**. Definition of voltage inputs corresponding to each logic gate TRUE and FALSE statement.

| Gate | Logic | Parameters   |               |  |
|------|-------|--------------|---------------|--|
|      |       | Voltage [mV] | Duration [ms] |  |
| AND  | FALSE | -500         | 500           |  |
|      | TRUE  | 1000         | 500           |  |
| OR   | FALSE | -500         | 500           |  |
|      | TRUE  | 2000         | 500           |  |
| NAND | FALSE | 500          | 500           |  |
|      | TRUE  | -1000        | 500           |  |
| NOR  | FALSE | 500          | 500           |  |
|      | TRUE  | -2000        | 500           |  |

Following each set of logical inputs, a "reset" sequence occurs where the previous input pulse pattern is driven at a reverse bias in order return the device back to the state prior to programming. For example, a A = TRUE and B = FALSE logic computation using the AND gate was initiated by passing a TRUE to the device with a +1000 mV, 500 ms pulse followed by a FALSE -500 mv, 500 ms pulse. After this sequence of pulses was sent to the G electrode, a current read of the channel was made that gave  $|i_{ds}| = 71.15 \ \mu$ A, an absolute value less than the baseline current and thus the computation resulted in a FALSE value. As **Figure 7**a indicates, the cPECM device exhibits logic computations for all the combinations of the A and B inputs that are consistent with an AND gate. The associative property to differing input values previously discussed is evident by the similarity of current outputs for input values that are either FALSE then TRUE or TRUE then FALSE.

The predictable and linear response to the sign, amplitude, and duration of the input voltage pulses (cf. **Figure 3**) allowed for the relatively straightforward determination of the sequence of pulses that must be applied to the cPECM to create a number of logic gates. The basic digital logic gates of AND and OR have TRUE outcomes for positive voltage impulses and FALSE outcomes for negative voltage impulses, while their negated equivalents of NAND and NOR have an opposite sign multiplied to their input pulses. The characteristics of the square-wave voltage pulses required to represent a TRUE or

FALSE value within a specific logic gate are presented in **Table 2**, while the logical computations for the OR, NAND, and NOR gate are presented in **Figures 7**b-d, respectively.



Figure 7. Boolean algebra: Logic gates a) AND, b) OR, c) NAND, and d) NOR.

Important considerations in the design of an artificial synapse are the voltage pulse magnitude/duration and energy requirements to trigger a synaptic event. Biological neuromor-phic systems achieve energy consumption per operation that is an extremely small amount of energy, on the order of 1-10 *fJ* per synaptic event. The cPECM device utilized in this study employs a large 12 x 20 mm active area with a 100  $\mu$ m spacing between the D and S electrodes. This model system could be quickly optimized to reduce device size and power requirements. For example, the consecutive changes in the resistance (synaptic events) were accomplished by an unoptimized ±500 mV pulse of 500 ms which has an energy requirement of ca. 42 *pJ* mm<sup>-2</sup> (E = V *x i x t* = 500 mV x 40 nA x 500 ms), though synaptic events could be programmed by lowering the voltage magnitude and impulse duration to ±50 mV pulse and 100 ms to give an energy requirement of approximately 0.31 *pJ* mm<sup>-2</sup>, an almost 100% drop in energy requirements. Recent advances in R2R printing have allowed for the reliable printing of 20  $\mu$ m structures with a minimum internal linewidth of 3  $\mu$ m at print speeds 0.2 m s<sup>-1</sup>.<sup>[37]</sup>

requirements on the order of 0.1 fJ for a 20  $\mu$ m device, a value similar to recently presented three-terminal artificial synapses.<sup>[14,47]</sup>

In summary, a fully water-soluble, self-doped PEDOT was synthesized and fabricated into electrochemical neuromorphic organic devices that demonstrates high conductivity linearity over 500 distinct states per potentiated or depressed cycle, low-energy consumption (0.31 pJ mm<sup>-2</sup>), and ease of scalability due to low-cost materials and fabrication techniques. Roll-to-roll (R2R) printing fabrication allowed for the ease of mass production of such devices that function as information storage and processing units with neuromorphic capabilities. This is a demonstration of the first steps towards the implementation of this device as an artificial neural network.

#### **3. Experimental Section**

*Materials*: All reagents were purchased from Alfa Aesar, TCI America, and used without further purification. All the solvents used for reactions were distilled under argon after drying over an appropriate drying reagent.

*Synthesis of Monomer S-EDOT:* sodium 4-((2,3-dihydrothieno [3,4-b] [1,4]dioxin-2-yl)methoxy)butane-2-sulfonate has been previously prepared in literature.<sup>[38]</sup>

Synthesis of Polymer S-PEDOT: S-EDOT (0.2 g, 0.61 mmol) was dissolved in deionized (DI) water (4 mL) then iron(III) chloride hexahydrate (0.1 g, 0.37 mmol) was added into solution. The obtained solution was stirred and degassed with nitrogen before an aqueous solution of sodium persulfate (0.33 g, 1.21 mmol in 4 mL of water) was added dropwise into the main solution under nitrogen. This mixture was stirred for 20 h at room temperature. After, the solution was diluted with water (4 mL) and treated with Amberlyst 15 cation exchange resin following by Diaion (WA30) anion exchange resin. The obtained solution was evaporated under vacuum to give a pure polymer. Yield 0.128 g (69%), dark blue paste.

Device Fabrication: Devices were fabricated on substrates of indium tin oxide (ITO)-coated polyethylene terephthalate (PET) (Aldrich Chemistry) with resistance of 60  $\Omega$  sq<sup>-1</sup>. Gate electrodes were templated using polyimide tape to mask the desired ITO electrode (12 mm wide). An acid-etch process is used to remove the unwanted ITO with hydrochloric acid (36%, VWR, CAS Number: 7647-01-0) and zinc powder (Fischer Scientific, CAS Number: 7440-66-6). The bottom electrodes are templated using HPR 504 photoresist (Arch Chemicals, Inc.) spin coated at 4000 RPM for 40 s using a Specialty Coating Systems Spincoat G3P-8 and annealed at 105 °C for 15 min on a hot plate prior to exposure of UV light using a Kepro UV model BTX-200A for 5 min with the appropriate lithography template. After phototemplating the pattern, the slides were developed with OPD 4262 (Arch Chemicals, Inc., CAS Number: 75-59-2) for 20 s before being rinsed with DI water. The films were dried at 105 °C for 15 min and then at 120 °C for 15 min. Once dried, the same acid-etch process as stated above was used to remove the unwanted ITO. The slides were then submerged in Microstripper 2001 (Arch Chemicals, Inc., CAS Number: 872-50-4) to remove the photo-etched HPR 504 film to expose the desired ITO pattern. In this work, the channel length between drain and source electrode was 100  $\mu$ m unless otherwise stated. Prior to any coating, all substrates were washed with DI water, acetone (Fischer) and isopropyl alcohol (Fischer) in a sonicator for 15 min each and then plasma cleaned in a Harrick PDC-32G plasma cleaner on high for 15 min.

The S-PEDOT polymer was coated from a 2:1 methanol:water solution at a concentration of 5 mg mL<sup>-1</sup>. Printing of devices was preformed on PET substrates with a RK K Printing Proofer attached with a

gravure head at a speed of approximately 0.2 m s<sup>-1</sup>. After coating, the bottom electrode was de-doped with an ionic conducting material, polyethylenimine (PEI) ( $M_w = 800$ , Sigma Aldrich, CAS Number: 25987-06-8), via vapor-doping at 250 °C for 8 min in a sealed chamber at atmospheric pressure. Using a KLA Tencor Step Height Profilometer, film thickness of the printed films for S-PEDOT and S-PEDOT:PEI were measured to be approximately 130 nm and 225 nm, respectively. To prepare the polymeric electrolyte gel, first a solution of 1.5 g tetrabutylammonium hexafluorophosphate ( $Bu_4NPF_6$ ) (Sigma Aldrich, CAS Number: 3109-63-5) was added to 20 mL of propylene carbonate (Acros, CAS Number: 108-32-7) and dissolved for 12 h. Then 500 µL of polyethylene glycol methacrylate (PEGMA) ( $M_n = 360$ , Aldrich, CAS Number: 25736-86-1), 50 µL of polyethylene glycol dimethacrylate (PEGDMA) ( $M_n = 550$ , Aldrich, CAS Number: 25852-47-5), and 5 µL of 2,2-diethoxyacetophenone (DEAP) (Fluka, CAS Number: 6175-45-7) were added to 1 mL solution of Bu4NPF6 in propylene carbonate and mixed. The electrolyte solution was vortexed prior to use. The top and the bottom substrates were sandwiched with a 125 pm thick parafilm spacer placed between the two PET sheets. The electrolyte solution was injected into the 12 x 20 mm space and photo-polymerized under a UV-light for 8 min per side in 2 min intervals using a ELC-500 Light Exposure System.

*Device Characterization*: Electrical characterization of the devices was done using a HP4145A Semiconductor Analyzer to apply the voltage- or current-pulse train to the gate electrode. A Keithley 2440 5a Sourcemeter was used to monitor the current across the drain and source channel electrodes. The HP4145A Semiconductor Analyzer was interpreted with custom HTBasic code and the Keithley 2440 5a Sourcemeter used LabView.

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