Power Source Unit of a Small Airship

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Abstract: - This paper describes a proposal on a construction of a power supply module that is intended to be implemented in a small airship. Because the bearing capacity of the airship is limited, simple and efficient voltage converters must be employed. The paper provides a description of a proposal on mutual timing of these converters that leads to eliminating of the interferences caused by the currents that are drawn by the converters. The hereby described method allows the designers to use smaller capacitors and inductors which will result in smaller weight and dimensions of the power supply unit. Furthermore, an example of a voltage converter design is provided in the framework of the paper.

Key-Words: Timing, Synchronization, Switched Voltage Converter, Airship, Interferences

1 Introduction

The design of power supply unit for a small airship offers several specific problems. As the load capacity of the airship is limited, including the weight of the battery, lightweight and power efficient solution must be applied. For this purpose, three parallel single-ended primary-inductor converters (SEPIC) are intended to be used, as this solution brings several advantages:

- The operation of SEPIC units can be hibernated anytime, just by stopping the oscillator. Regardless of whether the converter increases or decreases the voltage, when not running, the output is isolated from the input by a coupling capacitor. This is advantageous especially with step-up converters as conventional "boost" topology cannot simply break the connection between the input and output of the circuit.
- The SEPIC units can both decrease or increase the voltage. This feature is crucial when battery is employed as its voltage can vary in time and be higher or lower compared to the required output voltage.
- Although two inductors are needed for one voltage branch, they can be wounded on one core. Moreover, with the approach described in this paper, they can be made small and lightweight.
- As three different output voltages are required, three parallel converters are used. This approach enables to synchronize their switching in order the current drawn from the accumulator included large steady-stated component. Details are described below in this paper.

2 Problem Formulation

The block diagram of the designed power supply unit is described by Fig. 1. As the source of energy, the 7.2 V / 2.4 Ah Li-Pol battery is used.

The requirements on the power supply source are as follows:

- Direct power supply to the motors so that high efficiency was achieved,
- 3.3 V / 1 A output for RFID tags detectors and other optional modules,
- 5.0 V / 1 A output for the central microcontroller, ultrasonic detectors, WiFi router, IP relay Charon I, motor controller and other optional modules,
- 12.0 V / 0.5 A output for the IP camera.
- The accumulator must be protected from the deep discharge.

As the accumulator consists of two 3.6 V cells, the deep discharge protection must check the condition of both of them. The deep discharge

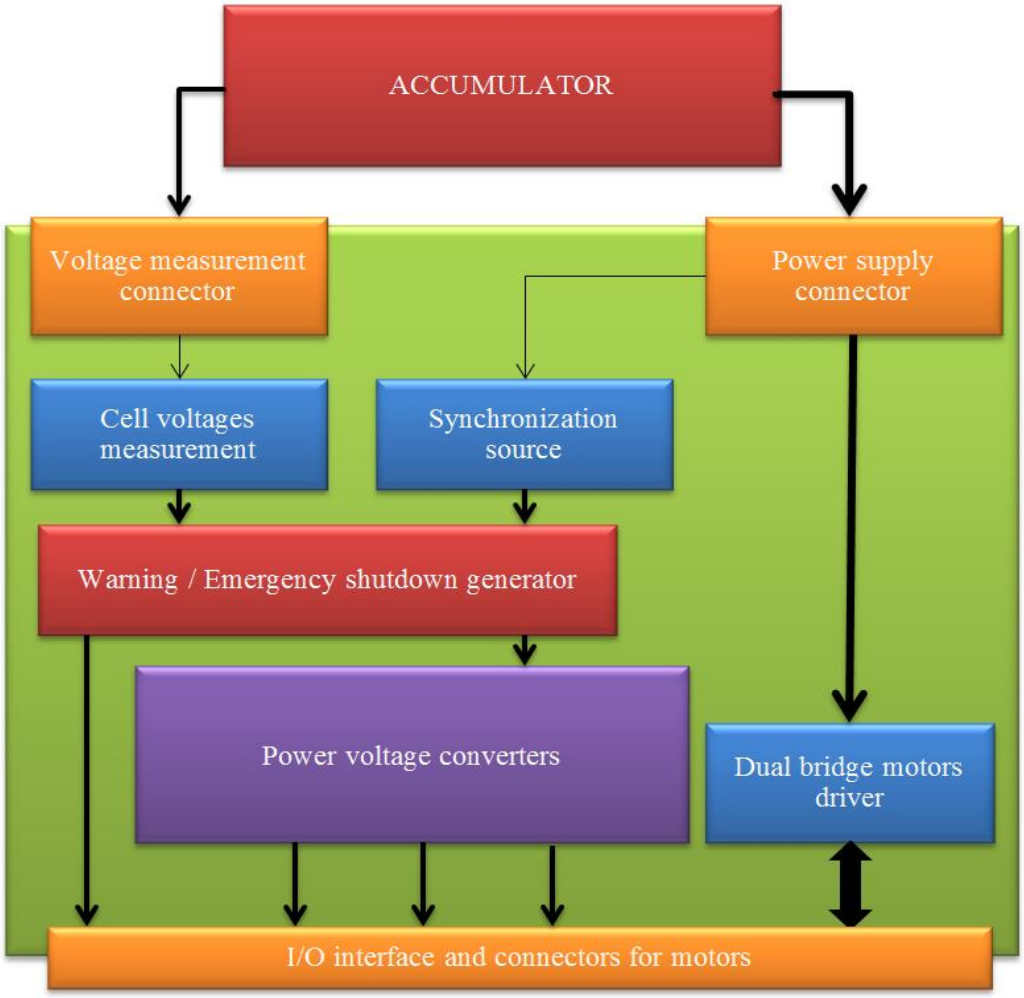

Fig. 1 – Airship's power supply unit block diagram

protection is expected to generate two types of signals:

- Warning – if the voltage of any of the cells drops below 3.0 V, the warning signal is generated. This signal is then processed by the controller of the Autonomous monitoring system. For example, on the basis of this signal the controlling algorithm can be switched to the mode that ensures that the Autonomous monitoring system returns to the starting point at which the accumulator can be charged or replaced.
- Emergency – if the voltage of any of the cells drops below 2.85 V, the emergency signal is generated, causing the disconnection of all circuits from the accumulator. In this case, the Autonomous monitoring system is in an "emergency off" state, and being uncontrolled, it descends to the ground by its own weight. This is because the cells of the accumulator can be irreversibly damaged in case their voltage drops below 2.75 V.

As depicted in the figure, the unit also includes motor drivers. The motor drivers are described in [7] and are not a subject to be described within the framework of this paper. The motor drivers are implemented in one unit in order to minimize the connections of power lines.

The accumulator is connected to the power supply board by means of cables – the power one and the voltage measurement supporting one. The power cable delivers the power to motors as well as well as to three switched-mode operating power supply voltage regulators. The voltage measurement cable supplies the low-power comparators that have the capability of generating the warning and emergency shutdown signals. While the warning signal is delivered to the output connector, the emergency

shutdown signal turns the voltage regulators off immediately. Once it occurs, the emergency shutdown signal can only be discontinued by disconnecting the accumulator. The synchronization of the SMPS controllers is provided by the synchronization block that ensures that the individual controllers are triggered at the defined moments, as described below.

3 Synchronization of the Converters

There are three different switched-mode operating voltage converters intended to be employed on the power supply board. It is convenient to make them operate synchronously in defined time shifts among their triggering pulses. All three voltage regulators are based on LT1172 voltage controllers [2]. These devices enable external synchronization and are suitable for SEPIC converters construction. Detailed information on their utilization can be found in [1].

When the parallel converters are triggered at different time periods, a sum of current ripples at the output of the accumulator can be obtained that shows a considerable DC component. In this chapter the synchronisation principle is described together with advantages it brings.

There is a set of equations below, according to which the duty cycles of all three voltage regulators can be estimated. The considerations are as follows:

- The duty cycles are estimated for minimum (5 V) and maximum (9 V) input voltage,
- The load of the voltage converters is "nominal", which means 1.0 A for 3.3 V and 5.0 V branch and 0.5 A for 12 V branch.
- The voltage drop on the Schottky diodes is $U_D = 0.4$ V.

$$D_{3.3V_{min}} = \frac{U_{OUT} + U_D}{U_{IN_{max}} + U_{OUT} + U_D} = \frac{3{,}3 + 0{,}4}{9 + 3{,}3 + 0{,}4} \approx 29\ \% \quad (1)$$

$$D_{3.3V_{max}} = \frac{U_{OUT} + U_D}{U_{IN_{min}} + U_{OUT} + U_D} = \frac{3{,}3 + 0{,}4}{5 + 3{,}3 + 0{,}4} \approx 43\ \% \quad (2)$$

$$D_{5V_{min}} = \frac{U_{OUT} + U_D}{U_{IN_{max}} + U_{OUT} + U_D} = \frac{5 + 0{,}4}{9 + 5 + 0{,}4} \approx 38\ \% \quad (3)$$

$$D_{5V_{max}} = \frac{U_{OUT} + U_D}{U_{IN_{min}} + U_{OUT} + U_D} = \frac{5 + 0{,}4}{5 + 5 + 0{,}4} \approx 52\ \% \quad (4)$$

$$D_{12V_{min}} = \frac{U_{OUT} + U_D}{U_{IN_{max}} + U_{OUT} + U_D} = \frac{12 + 0{,}4}{9 + 12 + 0{,}4} \approx 58\ \% \quad (5)$$

$$D_{12V_{max}} = \frac{U_{OUT} + U_D}{U_{IN_{min}} + U_{OUT} + U_D} = \frac{12 + 0{,}4}{5 + 12 + 0{,}4} \approx 73\ \% \quad (6)$$

The maximum current consumptions of the voltage regulators are estimated under the following conditions:

- The efficiency of the voltage converter is 85 %,
- The input voltage is 5 V (as low as possible according to specifications),
- The voltage regulators have to deliver nominal output currents.

$$I_{IN_{3,3V}} = I_{OUT} \cdot \frac{1}{\eta} \cdot \frac{U_{OUT}}{U_{IN}} = 1 \cdot \frac{1}{0{,}85} \cdot \frac{3{,}3}{5} \cong 0{,}78\ [A] \quad (7)$$

$$I_{IN_{5V}} = I_{OUT} \cdot \frac{1}{\eta} \cdot \frac{U_{OUT}}{U_{IN}} = 1 \cdot \frac{1}{0{,}85} \cdot \frac{5}{5} \cong 1{,}18\ [A] \quad (8)$$

$$I_{IN_{12V}} = I_{OUT} \cdot \frac{1}{\eta} \cdot \frac{U_{OUT}}{U_{IN}} = 0{,}5 \cdot \frac{1}{0{,}85} \cdot \frac{12}{5} \cong 1{,}41\ [A] \quad (9)$$

Furthermore, if the operating frequency of the voltage regulators is estimated to be up to 125 kHz (the period T = 8 µs) and the current ripple is estimated to be up to ± 40 %, the currents flowing into the appropriate voltage converters can be described by appropriate equations.

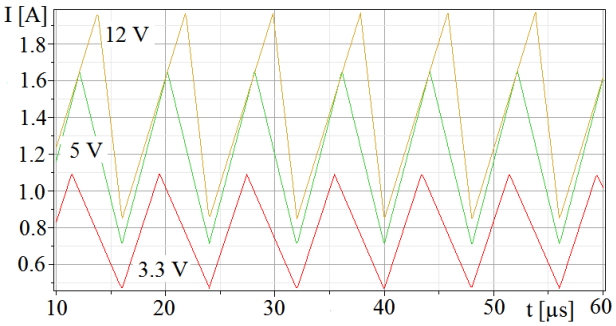

Fig. 2 – Currents drawn by the power supply unit when all three channels are triggered at the same time

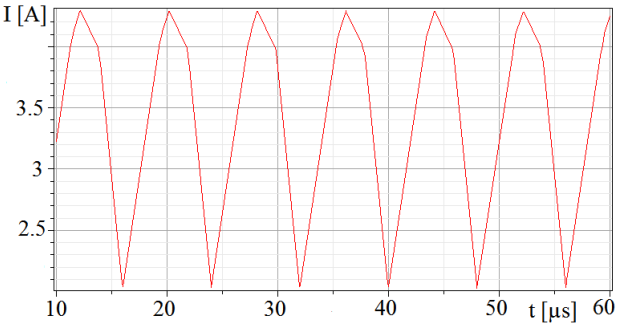

Fig. 3 – Sum of the currents drawn by the power supply unit when all three channels are triggered at the same time

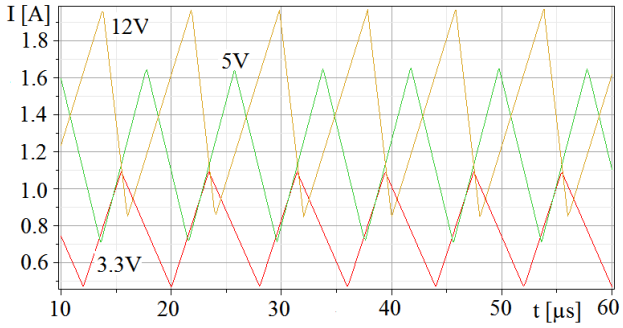

Fig. 4 - Currents drawn by the power supply unit when shifted triggering is applied

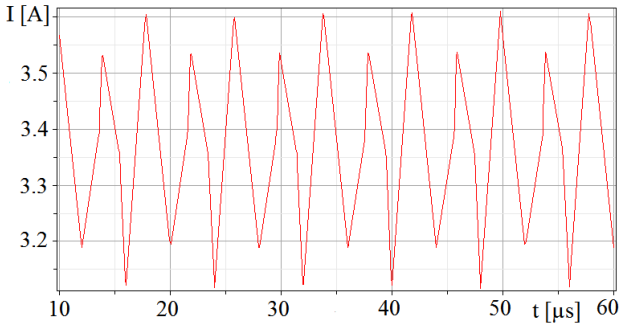

Fig. 5 – Sum of the currents drawn by the power supply unit when shifted triggering is applied

The current waveforms described by the equations were analysed in the Maple software. In the figures below the currents flowing into the particular voltage converters are depicted as well as their sum for two cases. The first case is described by figures 2 and 3 shows how these currents look like if all the converters are triggered at once while the second case, described by the figures 4 and 5, shows the situation that occurs when the converters are triggered in mutually shifted periods.

Based on the above pictures the following conclusions can be made: If the triggering of the voltage converters is not optimized, the pulse component of the current drawn from the accumulator can be up to $\Delta I = 2.3$ A. Moreover, it is obvious that the current ripple is mostly caused by the 12 V and 5 V branches. Therefore, it is convenient to shift the triggering time of the 5 V branch in such a way so that the maximum peak in the 5 V branch meets the minimum peak in the 12 V branch. Obviously, there is a need to find a compromise that allows simple construction of the triggering circuit. For the purpose of this paper dividing the period of the converters operation by ten was chosen. The tenths of the basic clock signal can be generated simply by the Johnson's counter. The following time shifts were defined, with respect to the expected operating frequency of 125 kHz, by modelling in Maple software:

- 12 V branch voltage converter is triggered in $t = (nT + 0)$ µs,
- 5 V branch voltage converter is triggered in $t = (nT + 2.4)$ µs,
- 3.3 V branch voltage converter is triggered in $t = (nT + 4.0)$ µs.

The resulting waveforms are depicted in Fig. 4. In Fig. 5 the waveform of the current drawn from the accumulator is depicted. It is obvious that the pulse component is lowered from $\Delta I = 2.3$ A to $\Delta I' = 0.5$ A, thus by 78 %. In practice, the effective decrease of the pulse component will be lower because the timing of the voltage converters is fixed and does not reflect the load or input voltage variability. This is a compromise between simple construction and ideal conditions. Nevertheless, every decrease of the pulse component in the current drawn by the voltage converters brings the following positive effects:

- The pulse load on the accumulator is declined, resulting in its higher lifetime,
- The pulse component of the drawn current flowing through the cable between the accumulator and the power supply board is decreased, which results in lower emitting of interfering electromagnetic field.
- The pulse current through the decoupling capacitor on the power supply board is decreased, which has several positive effects:
  - The capacity of the decoupling capacitor can be lower,
  - The capacitor is subjected to a smaller ripple current, which results in its higher lifetime.

Furthermore, the amount of the pulse component was modelled for the above mentioned triggering for the cases in which the loads of the voltage converters are still nominal, but the accumulator voltage varies in the following steps: 5, 6, 7, 8 and 9 V. Fig. 6 depicts the level of the pulse component at these voltages for the case of triggering at the same time and for the case of shifted triggering. The calculated points are interleaved with a curve base on the 4th order polynomial. It can be observed that the pulse component of the current drawn from the accumulator is decreased at any supply voltage.

The modelling was done for the nominal loads of the voltage regulators, because it was expected that under less loads the supply current would also be lesser, resulting in the smaller pulse component.

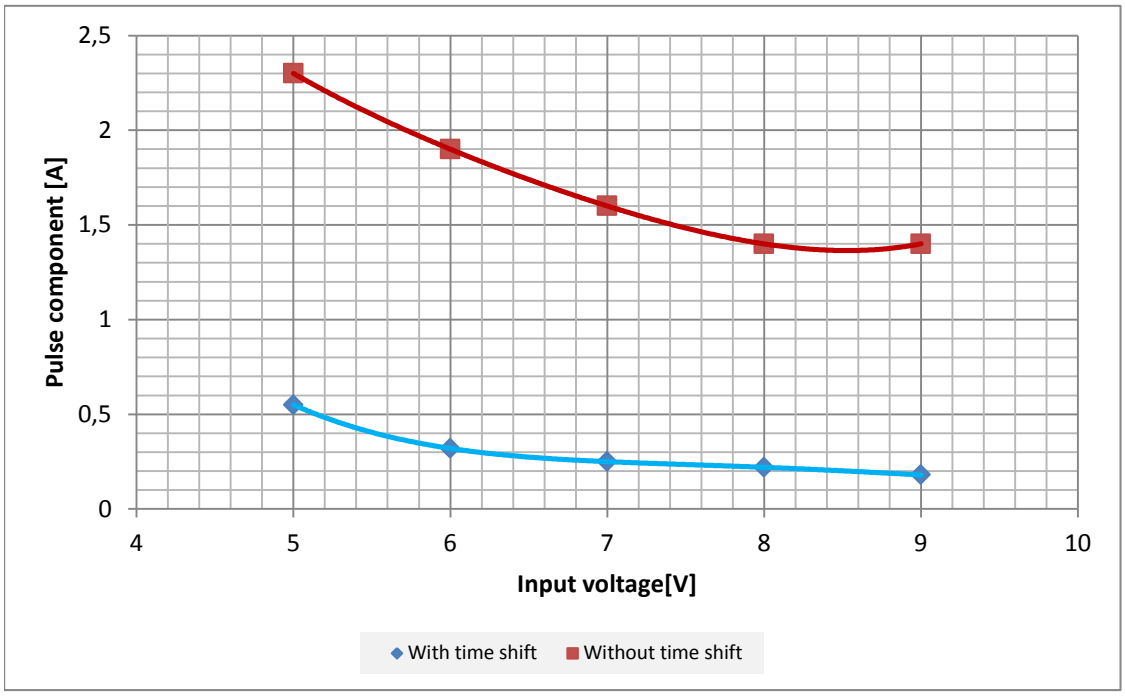

Fig. 6 – Comparison of the pulse components in the current drawn from the accumulator

Furthermore, by applying progressive time shift instead of fixed time delays, the pulse currents could be eliminated more properly.

4 SEPIC Converters Proposal

As previously stated, there are three different voltage regulators operating in the switched mode. The regulators are all based on the LT1172 controllers and their topology is also identical. They differ only in the device values. Therefore, in the text below only a design of the 5V branch voltage regulator is described in details. For two other regulators only additional notes are provided.

The design is based on the SEPIC topology, utilizing the information given by the manufacturer of the LT1172 chips in the appropriate datasheet [2]. Although in comparison with other topologies the efficiency of the SEPIC voltage converters is lower, they were chosen for their following advantages:

- The output of the voltage regulator is always disconnected for DC currents when the regulator is not clocked.
- The output voltage can be lower or higher than the input voltage in the same topology.
- The output polarity is not inverted.

The basic circuit diagram of the voltage regulator was simulated in LT Spice IV software. This is a freeware circuit simulator based on SPICE libraries, modified by the LT1172 manufacturer. Unfortunately, the external synchronization cannot be simulated here. Only the 100 kHz internal oscillator embedded in the chip is utilized. Moreover, there are some features of the controller that are simultaneously controlled via its V_C pin and not all of them can be simulated at once. These functions are as follows:

- Soft start
- Overcurrent protection
- Synchronization

The overcurrent protection and soft start functionality are tied together as the maximum current through the accumulating inductor is limited by the voltage at the VC pin. Unfortunately, the peak values of the current through the inductor depend not only on the output current of the converter but it is inversely proportional to the supply voltage as well.

The basic simulation diagram of the 5V converter is depicted in Fig. 7. The device values were determined according to the following computations and assumptions.

The Schottky diode D1 is MBRS340. Its reverse breakdown voltage is up to 40 V and its forward voltage is expected to be at least 0.4 V. According to (3) and (4), the duty cycle at the maximum load can vary from approximately 38 % to approximately 52 %. The maximum allowed current ripple at the inductors was considered to be no higher than ±15

%, thus 30 %. The ripple current can be expressed as follows:

$$\Delta I_L = I_{OUT} \cdot \frac{U_{OUT}}{U_{IN(min)}} \cdot 30\% = 1 \cdot \frac{5}{5} \cdot 0.3 = 0.3\ [A] \quad (10)$$

According to this knowledge the minimum inductance of the inductors can be calculated:

$$L_{min} = \frac{U_{IN(min)}}{\Delta I_L \cdot f_{sw}} \cdot D_{(max)} = \frac{5}{0.3 \cdot 10^5} \cdot 0{,}52 = 3.25 \cdot 10^{-5} = 86.7\ [\mu H] \quad (11)$$

Unfortunately, the simulator does not support the simulation of the externally synchronized circuit operating at the frequency of 125 kHz. Instead, only 100 kHz operating frequency is expected. Therefore, the f_{SW} parameter was considered to be 100 kHz. However, it is reasonable to choose one of the standardized inductor values. Moreover, according to (11) the minimum required inductance is inversely proportional to the operating frequency f_{SW}. Let us therefore consider the application of 100 µH inductors in the real application that are replaced by 125 µH inductors for the purpose of the simulations. Then the peak currents in the simulation will be equal to the peak currents obtained in the real circuits. The calculation of the peak currents is as follows:

$$I_{L1(peak)} = I_{OUT} \cdot \frac{V_{OUT} + V_D}{V_{IN(min)}} \cdot \left(1 + \frac{30\%}{2}\right) = 1 \cdot \frac{5 + 0.4}{5} \cdot 1.15 = 1.24\ [A] \quad (12)$$

$$I_{L2(peak)} = I_{OUT} \cdot \left(1 + \frac{30\%}{2}\right) = 1.15\ [A] \quad (13)$$

In practical realization both inductors can be made on one core because their magnetic fluxes are synchronous and approximately of the same value. Moreover, their value can be decreased to 2 x 50 µH, resulting in better efficiency due to their lower serial resistance. The serial resistance of the inductors in the simulation diagram was considered to be up to 0.1 Ω.

The coupling capacitors C1 and C5 shall be of a good quality and low-ESR type. These capacitors are loaded with current as follows:

$$I_{C(rms)} = I_{OUT} \cdot \sqrt{\frac{U_{OUT} + U_D}{U_{IN(min)}}} = 1.04\ [A] \quad (14)$$

Tantal capacitors with the voltage rating of 16 V will be sufficient for this application. Their capacity can be determined as follows:

$$C_s = \frac{I_{OUT} \cdot D_{max}}{\Delta U_{Cs} \cdot f_{sw}} = \frac{1 \cdot 0.52}{2.5 \cdot 10^5} = 2.08\ [\mu F] \quad (15)$$

The ΔU_{Cs} parameter refers to the voltage ripple at the capacitors and for the purposes of this design it was expected that:

$$\Delta U_{Cs} \leq 0.5\ U_{IN(min)} \quad (16)$$

In order increase the efficiency of the converter, two 2.2 µF capacitors connected in parallel are considered.

The maximum voltage ripple at the output of the converter is expected to be at least 50 mV. Mainly the serial resistance of the filtering capacitors is critical. It can be determined as follows:

$$ESR \leq \frac{U_{ripple} \cdot 0{,}5}{I_{L1(peak)} + I_{L2(peak)}} = \frac{0.05 \cdot 0.5}{2{,}39} \cong 0.01\ [\Omega] \quad (17)$$

This implies that more filtering capacitors connected in parallel must be used. However, such a small ESR cannot be achieved in practice because of the finite conductivity of the printed circuit board copper clad.

The capacity of the filtering capacitor(s) can be calculated as follows[1]:

$$C_{OUT} \geq \frac{I_{OUT} \cdot D_{max}}{0.5 \cdot U_{ripple} \cdot f_{sw}} = \frac{0.52}{0.5 \cdot 0.05 \cdot 10^5} = 207.6\ [\mu F] \quad (18)$$

In practical realization, four 47 µF capacitors will be employed being amended with 4.7 µF tantal capacitor and 100 nF ceramic capacitor, all connected in parallel.

The internal voltage reference is stabilized to 1.25 V. Therefore, in order to limit the output voltage to 5 V, the voltage dividers R1 and R2 ensuring the voltage feedback must divide the output voltage by 4. The values R1 = 100 kΩ and R2 = 33 kΩ are perfect for this purpose.

[1] Again, f_{SW} = 100 kHz instead of f_{SW} = 125 kHz is considered as explained in the text above. In this case the effect of this change will probably be negligible due to the fact that the ESR practically cannot be as small as possible and the error caused by the real ESR value will be much higher than the error caused by the change of the f_{SW} parameter.

In the following paragraphs a design of indirect current limitation feedback is described. As stated in the description of the LT1172 chip, the current limitation is set internally to the peak current of 2 A and can be adjusted by decreasing the voltage at the Vc pin of the chip. In order to avoid affecting the efficiency of the converter it was decided to measure the output current indirectly from the peak current flowing through the inductors. However, not only is this current proportional to the output current but it also is inversely proportional to the input voltage, being additionally affected by the change of the ripple current due to the change of the duty cycle of the converter. Therefore, at least two peak currents at different input voltages must be known.
Let us choose the maximum and the minimum input voltage and calculate the peak currents obtained by the circuit devices described in the text above. Because the inductors are expected to be of higher inductance than calculated, new calculations of the ripple current are needed[2]:

$$L = \frac{U_{IN}}{\Delta I_L \cdot f_{sw}} \cdot D \Rightarrow \Delta I_L = \frac{U_{IN}}{L \cdot f_{sw}} \cdot D \quad (19)$$

$$\Delta I_L(9V) = \frac{9}{1.25 \cdot 10^{-4} \cdot 10^5} . 0.38 = 0.27\ [A] \quad (20)$$

$$\Delta I_L(5V) = \frac{5}{1.25 \cdot 10^{-4} \cdot 10^5} . 0.52 = 0.15\ [A] \quad (21)$$

The percentage value of the ripple R can then be determined as follows:

$$\Delta I_L = I_{OUT} \cdot \frac{U_{OUT}}{U_{IN}} \cdot \frac{R}{100} \Rightarrow R = 100 \cdot \frac{\Delta I_L . U_{IN}}{I_{OUT} \cdot U_{OUT}} \quad (22)$$

$$R\ (9V) = 100 \cdot \frac{0.27 \cdot 9}{1 \cdot 5} = 48.6\ \% \quad (23)$$

$$R\ (5V) = 100 \cdot \frac{0.15 \cdot 5}{1 \cdot 5} = 15\ \% \quad (24)$$

It must be noted that the above mentioned calculations are only approximate, not considering the influence of the Schottky diode, coupling capacitors, serial resistances, switch saturation voltage etc.

Subsequently, the peak currents can be estimated as follows:

$$I_{L1(peak)} = I_{OUT} \cdot \frac{U_{OUT} + U_D}{U_{IN}} \cdot \left(1 + \frac{R}{200}\right) \quad (25)$$

$$I_{L1(peak)}(9V) = 1 \cdot \frac{5 + 0.4}{9} \cdot \left(1 + \frac{48.6}{200}\right) = 0.75\ [A] \quad (26)$$

$$I_{L1(peak)}(5V) = 1 \cdot \frac{5 + 0.4}{5} \cdot \left(1 + \frac{15}{200}\right) = 1.16\ [A] \quad (27)$$

According to the datasheet [2], the control voltage to switch current transconductance of the LT1172 is 2 A/V. The simulation shown that if the switched current is 0.9 A, the relevant Vc voltage is 1.8 V. This implies that in an "idle" state when no current is drawn the bias at the Vc pin is approximately 1.3 V and this voltage is increased proportionally to the output current. The maximum Vc pin voltage is 2.0 V, referring to the maximum switched current of approximately 1.4 A[3]. This can be expressed as follows:

$$U_{Vc} \cong 1.3 + 0.5\ I_{L1(peak)}\ [V] \quad (28)$$

This implies that the input voltage compensating circuit must ensure that the voltage at the Vc pin is limited to approximately 1.68 V if the input voltage is 9 V and to 1.88 V if the input voltage is 5 V. Beside the necessary bias, the gain of this circuit must be as follows:

$$A = \frac{U_{OUT\ high} - U_{OUT\ low}}{U_{IN\ high} - U_{IN\ low}} = \frac{-0.2}{4} = -0.05 \quad (29)$$

The bias must take into account the forward voltage of the coupling diode and the bias of the Vc pin. Utilizing the 1N4148 small-signal diode, at low currents that are sufficient to activate the Vc pin, its forward voltage can be considered at least 0.5 V. The total bias must then be set to approximately U_{BIAS} = 0.8 V. It is worth noting that by changing the bias voltage the current limit is being adjusted. Therefore, the inaccuracies in the calculations can be compensated by employing one trimmer adjusting the bias voltage.

[2] Assuming the duty cycles are D = 38 % @ 9 V and D = 52 % @ 5 V

[3] The LT1172 manufacturer guarantees the maximum switched current between 1.25 and 3.5 A provided the duty cycle is 50 %.

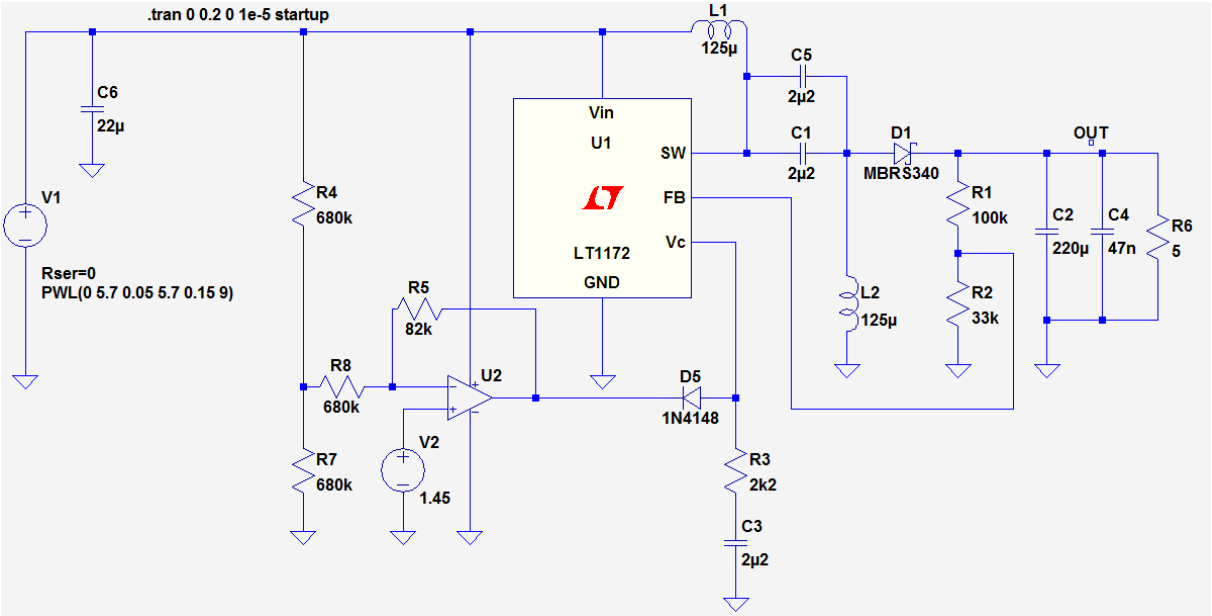

Fig. 7 – Basic circuit diagram for 5V voltage regulator simulation (LT Spice)

The compensating circuit is based on the U_2 operational amplifier and its behaviour can be described as follows. The superposition principle makes it possible to analyse the circuit separately for the inverting and the non-inverting input of the operational amplifier. Then the output voltage of the operational amplifier can be described as follows:

$$U_{OUT} = U_{OUT}^{+} + U_{OUT}^{-} \tag{30}$$

The + and – signs refer to the contributions of the non-inverting (+) and the inverting (-) input. The circuit can then be described separately, assuming the following conditions:

- The U^+ voltage is expressed as the contribution to the output of the circuit in case the non-inverting input is driven while the source connected to the inverting input is of zero voltage.
- The U^- voltage is expressed as the contribution to the output of the circuit in case the inverting input is driven while the source connected to the non-inverting input is of zero voltage.

Then the behaviour of the circuit can be described by the following equations:

$$U_{OUT}^{-} = -U_{IN} \cdot \frac{\frac{R7 \cdot R8}{R7 + R8}}{R4 + \frac{R7 \cdot R8}{R7 + R8}} \cdot \frac{R5}{R8} \tag{31}$$

$$U_{OUT}^{+} = U_{BIAS} \cdot \left(1 + \frac{R5}{R8 + \frac{R7 \cdot R4}{R7 + R4}}\right) \tag{32}$$

$$U_{OUT} = U_{BIAS} \cdot \left(1 + \frac{R5}{R8 + \frac{R7 \cdot R4}{R7 + R4}}\right) - U_{IN} \cdot \frac{\frac{R7 \cdot R8}{R7 + R8}}{R4 + \frac{R7 \cdot R8}{R7 + R8}} \cdot \frac{R5}{R8} \tag{33}$$

The voltage divider R4, R7 decreases the input voltage that can occur at the inverting input of the operational amplifier. As the FET based operational amplifier is expected to be employed, the current flowing through the divider can be very small. In order to simplify the calculations it is reasonable to choose the resistors R4, R7 and R8 of the same value. The following values can be chosen: R4 = R7 = R8 = 680 kΩ. This will simplify the (33) expression to the following state:

$$U_{OUT} = U_{BIAS} \cdot \left(1 + \frac{R5}{1.02 \cdot 10^6}\right) - U_{IN} \cdot 0.33 \cdot \frac{R5}{3.4 \cdot 10^5} \tag{34}$$

Beside the bias, the R5 resistor must be set according to the requirement resulting from the equation (33):

$$\Delta U_{OUT} = -0.05 \cdot \Delta U_{IN}$$
$$\Rightarrow \frac{\Delta U_{OUT}}{\Delta U_{IN}} = 0.33 \cdot \frac{R5}{3.4 \cdot 10^5} = 0.05$$
$$\Rightarrow R5 \cong 51\ [k\Omega] \qquad (35)$$

Now the bias voltage can be determined as well under the assumption that when the input voltage is 5 V, the required output voltage of the circuit is 1.88 - 0.5 = 1.38 V[4]:

$$U_{OUT} = 1.05 \cdot U_{BIAS} - 0.05 \cdot U_{IN}$$

$$\Rightarrow U_{BIAS} = \frac{U_{OUT} + 0.05 \cdot U_{IN}}{1.05} = 1.55\ [V] \qquad (36)$$

On completion the above mentioned calculations, the circuit was simulated. According to results of simulations only the value of the resistor R5 was increased from 51 to 82 kΩ and consequently the bias voltage was decreased from 1.55 to 1.45 V. This modification covered the inaccuracies that occurred in the calculations as a result of neglecting a greater amount of minor or parasitic parameters of the utilized devices.

The final simulations of the 5V regulator were processed for the input voltage varying from 5.7 V to 9 V. The minimum value is given by the theoretical minimum input operating voltage at which the Emergency shutdown circuit should suspend the operation of the power supply source. The maximum value is expected not to exceed 9 V for the 7.2V accumulator that is assumed to be employed. As the nominal output voltage is 5 V, the 5 Ω load resistor refers to the load that consumes 1 A.

The behaviour of the circuit including the load realized by the 5Ω resistor is depicted in Fig. 8.

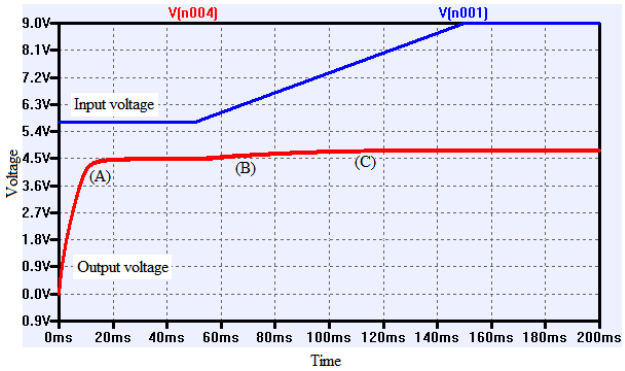

Fig. 8 – Simulation results of the circuit from Fig. 73 for different input voltage and 5Ω load

[4] It is necessary to calculate the voltage drop at the coupling diode.

Unfortunately, at the maximum expected load the circuit is not capable of delivering sufficient power. This is caused by the fact that the internal overcurrent protection of the chip is active at low voltages. In the Fig. 8 the following phenomena can be observed: the input voltage is fixed at the lowest level in the first 50 ms. Then it is raised to the maximum value at which it stays until the end of the simulation. The Output voltage curve refers to the output voltage of the voltage converter. There are three interesting points of this curve, marked by the letters (A), (B) and (C). From the end to the point (A) the soft start ramp is active. The time in which the converter starts to deliver the maximum output power is determined by the serial combination of R3 and C3 devices. Their values were set according to the recommendation of the manufacturer of the chip. When the soft start period finishes, the output voltage is stabilized to approximately 4.5 V, referring to the output current of 0.9 A. The nominal output voltage is not achieved due to the overcurrent protection implemented in the chip that does not allow to exceed the switching current of 1.25 A[5]. Even though, this may seem to be too strict in the simulation, but in practice the manufacturer guarantees the switching current to lie within 1.25 and 3.5 A. From the point (C) the output voltage is stabilized to approximately 4.8 V. From this point the external current limiting is active, setting the current limit to 0.96 A. Unfortunately, for this kind of chip and the indirect current sensing the overcurrent protection characteristics are quite weak, resulting in the fact that the threshold of the overcurrent protection migrates according to the load resistance.

Additional simulations were processed assuming the same configuration except the load resistance. The load resistance was set to 10 and 2.5 Ω. The results are depicted in Fig. 9 and Fig. 10. From the results of these it is obvious that the voltage converter operates properly. With the output current of 0.5 A the output voltage is precisely stabilized to 5.0 V and with the overloaded output the output voltage is approximately 2.9 V, referring to the output current of 1.16 A.

The Fig. 11 shows how the output voltage depends on the current drawn by the load provided the input voltage is of some nominal value, e.g. 7.2 V. For the nominal output current of 1 A the drop of the output

[5] According to the calculations, the current of 1.25 A would never be exceeded. However, many factors are neglected in the calculations, for example the serial resistances of the devices, the saturation voltage of the power switch etc.

voltage is approximately 10 %. This value can be adjusted by tuning the U_{BIAS} voltage.

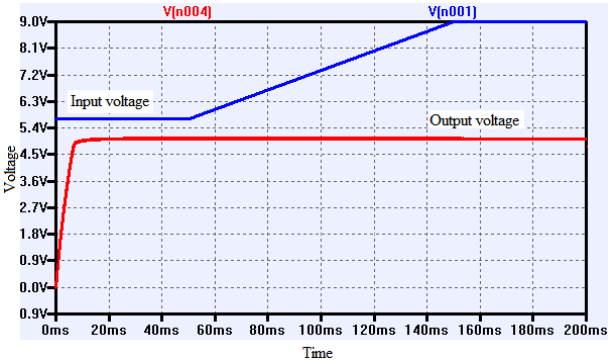

Fig. 9 – Simulation results of the circuit from Fig. 7 for different input voltage and 10Ω load

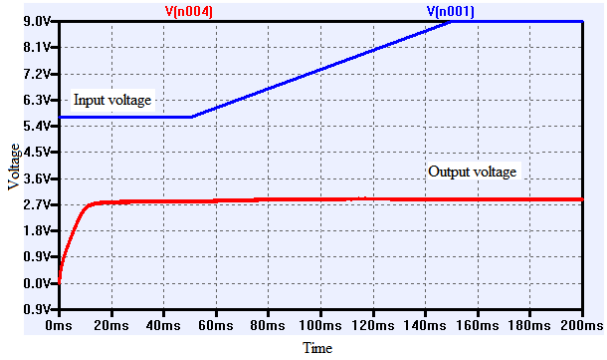

Fig. 10 – Simulation results of the circuit from Fig. 7 for different input voltage and 2.5Ω load

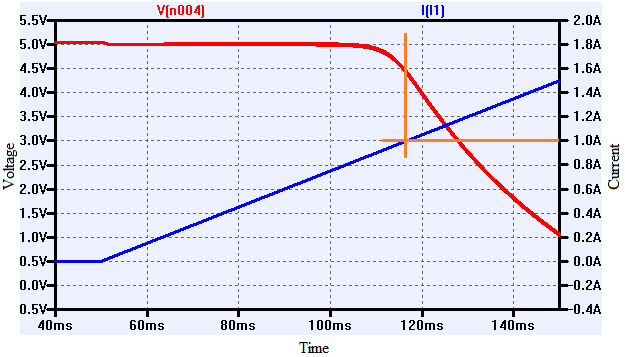

Fig. 11 – Simulation results of the circuit from Fig. 7 for different output current I(1).

However, it is obvious that the current limiting is quite soft and such adjustment will increase the shorted circuit current limit. Provided the values of the devices are as described in this paper, the short circuit current will not exceed 1.75 A.

In Fig. 12 the current through the L1 inductor is depicted provided the input voltage is 7.2 V and the output current is 1 A. The peak current is 0.87 A.

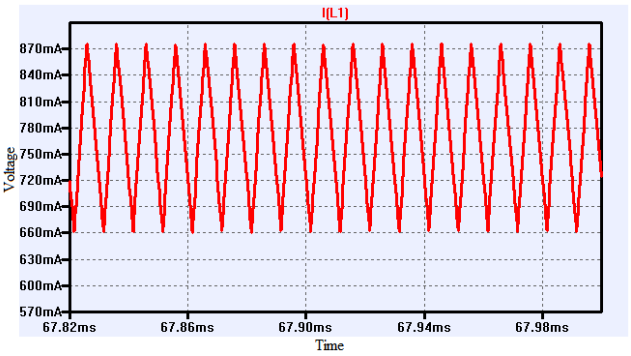

Fig. 12 – Simulation results of the circuit from Fig. 7 - waveform of the current passing through L1 inductor at the output current of 1 A and input voltage of 7.2 V

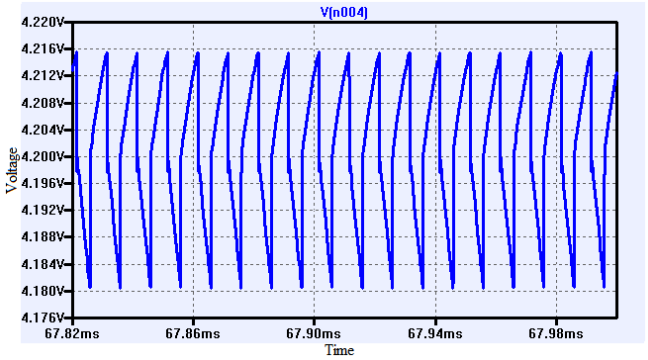

Fig. 13 – Simulation results of the circuit from Fig. 7 – voltage ripple at the output of the converter at the output current of 1 A and input voltage of 7.2 V

In Fig. 13 the ripple voltage at the output of the voltage converter is depicted provided the output is loaded with the current of 1 A and the input is fed by the nominal voltage of 7.2 V. The ripple voltage is 36 mV provided the ESR of the filtering capacitor is at least 0.01 Ω. This refers to the relative ripple of 0.85 %.

4 Conclusion

The paper describes a proposal on a construction of a power supply unit for a small airship. The unit is intended to deliver the power to the circuitry of Autonomous Monitoring System described in [3]. It shows that when there are more voltage converters operating in parallel, it is possible to synchronize them in the way to decrease the electromagnetic interferences caused by pulse currents.

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